The LNS ALU Parameters

19-bit LNS ALU

laddsub_19

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	8	112 MHz	684 (2%)	6 (4%)	192 (1%)
v2000e-6	8	70 MHz	808 (4%)	6 (4%)	192 (1%)

lmul_19
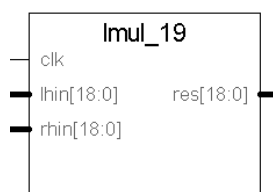
Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	140 MHz	58 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	81 MHz	56 (>1%)	0 (0%)	0 (0%)

ldiv_19

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	136 MHz	51 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	79 MHz	47 (>1%)	0 (0%)	0 (0%)

lsqrt_19

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	137 MHz	16 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	100 MHz	17 (>1%)	0 (0%)	0 (0%)

The LNS ALU Parameters

lmule_19

```
         lmule_19
   clk
   lhin[18:0]      res[18:0]
   rhin[18:0]
```
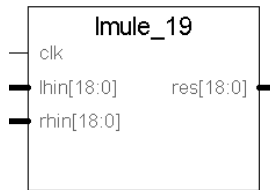
Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	136 MHz	45 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	89 MHz	47 (>1%)	0 (0%)	0 (0%)

ldive_19

```
         ldive_19
   clk
   lhin[18:0]      res[18:0]
   rhin[18:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	137 MHz	41 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	83 MHz	39 (>1%)	0 (0%)	0 (0%)

lsqrte_19

```
         lsqrte_19
   clk
                  res[18:0]
   din[18:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	155 MHz	23 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	100 MHz	24 (>1%)	0 (0%)	0 (0%)

ldnor_19

```
         ldnor_19
   clk
                  res[18:0]
   din[18:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	134 MHz	28 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	103 MHz	27 (>1%)	0 (0%)	0 (0%)

ilcnv_19

```
         ilcnv_19
   clk              rdy_il
   en_il            rdy_li
   en_li            rfd_il
                    rfd_li
   din_il[31:0]
                  dout_il[18:0]
   din_li[18:0]
                  dout_li[31:0]
```
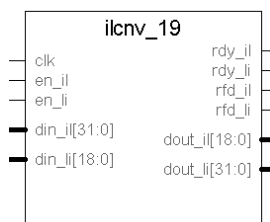
Device	CLK rate	int ⇒ log		log ⇒ int	
		lat.	RFD	lat.	RFD
2v1000-4	75 MHz *)	10	every 1	28	every 9
v2000e-6	53 MHz *)	10	every 1	28	every 9

*) module in testing design, uses laddsub_19

32-bit LNS ALU

laddsub_32

```
         laddsub_32
  ─ clk
  ─ suba
  ─ subb
  ─▶ lhina[31:0]    resa[31:0] ─▶
  ─▶ lhinb[31:0]    resb[31:0] ─▶
  ─▶ rhina[31:0]
  ─▶ rhinb[31:0]
```
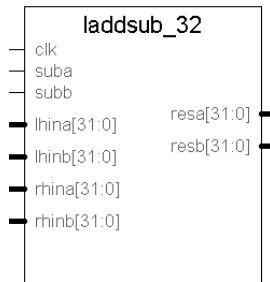
Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	8	97 MHz	1075 (3%)	28 (18%)	1280 (8%)
v2000e-6	8	65 MHz	1400 (7%)	96 (67%)	1280 (7%)

lmul_32

```
         lmul_32
  ─ clk
  ─▶ lhin[31:0]    res[31:0] ─▶
  ─▶ rhin[31:0]
```
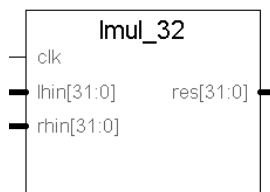
Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	140 MHz	83 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	72 MHz	85 (>1%)	0 (0%)	0 (0%)

ldiv_32

```
         ldiv_32
  ─ clk
  ─▶ lhin[31:0]    res[31:0] ─▶
  ─▶ rhin[31:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	138 MHz	79 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	74 MHz	80 (>1%)	0 (0%)	0 (0%)

lsqrt_32

```
         lsqrt_32
  ─ clk
                   res[31:0] ─▶
  ─▶ din[31:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	147 MHz	27 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	110 MHz	28 (>1%)	0 (0%)	0 (0%)

lmule_32

```
        lmule_32
─ clk
─ lhin[31:0]      res[31:0] ─
─ rhin[31:0]
```
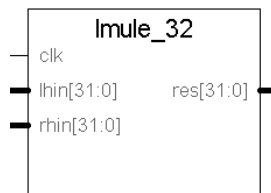
Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	138 MHz	67 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	66 MHz	67 (>1%)	0 (0%)	0 (0%)

ldive_32

```
        ldive_32
─ clk
─ lhin[31:0]      res[31:0] ─
─ rhin[31:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	141 MHz	63 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	74 MHz	64 (>1%)	0 (0%)	0 (0%)

lsqrte_32

```
        lsqrte_32
─ clk
            res[31:0] ─
─ din[31:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	143 MHz	36 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	108 MHz	36 (>1%)	0 (0%)	0 (0%)

ldnor_32

```
        ldnor_32
─ clk
            res[31:0] ─
─ din[31:0]
```

Device	lat.	CLK rate	SLICEs	BRAMs	TBUFs
2v6000-6	1	146 MHz	44 (>1%)	0 (0%)	0 (0%)
v2000e-6	1	105 MHz	44 (>1%)	0 (0%)	0 (0%)

SIGNAL PROCESSING