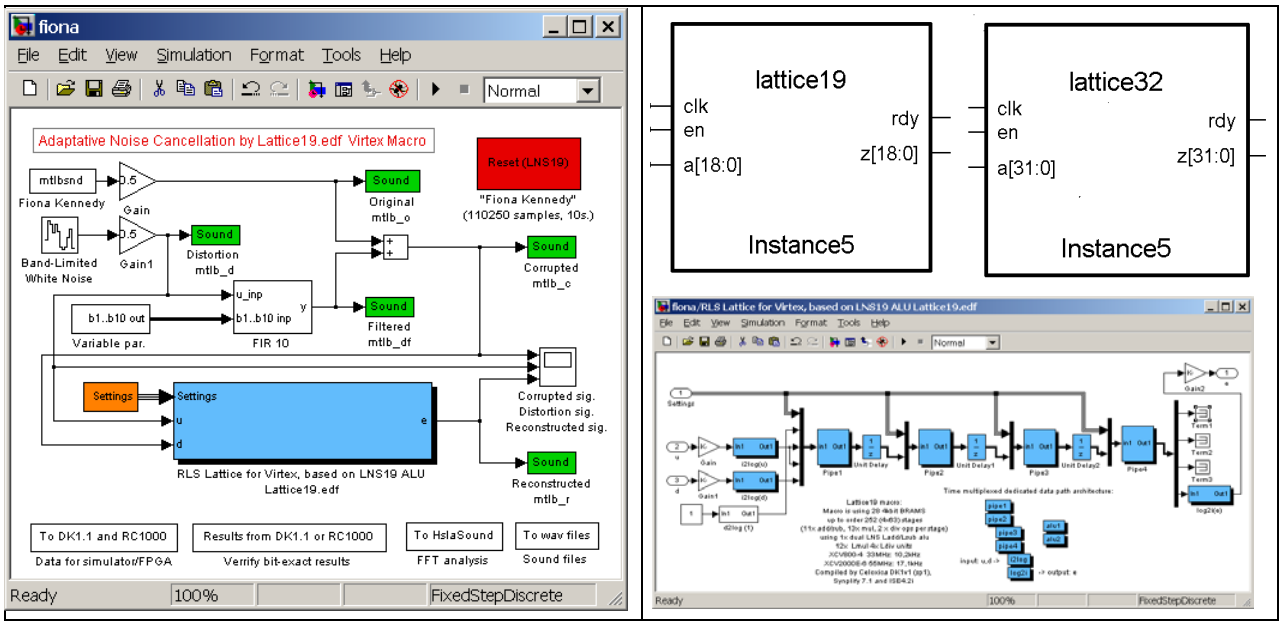
Adaptive Recursive Least Squares Lattice Filter

- For **active noise cancellation**, **hands free telephony**, **adaptive filters in intelligent sensors**.
- Adaptive Recursive Least Squares (RLS) Lattice filter in 19- or 32-bit Logarithmic arithmetic.
- Filter order programmable from 4 to 252.
- Programmable adaptation rate.
- Tested performance of XILINX Virtex implementations compared to TI C6711 floating point DSP:

Comparison of the maximal sampling frequency (RLS Lattice order 252)									
XILINX Virtex FPGA					***TI C67:***		*No. of chan.*	***XILINX Virtex*** *(kHz)*	***TI C67*** *(kHz)*
Type	*grade*	*clock*	*resources used*	*LNS prec.*	*Clock*	*Float prec.*			
XC2V2000	-6	84 MHz	(90% Slices 73% BRAMs)	32 bit	225MHz	32 bit	1	26,1	1,7
XCV2000E	-6	45 MHz	(55% Slices 76% BRAMs)	32 bit	167MHz	32 bit	1	13,6	1,3
XCV2000E	-6	52 MHz	(67% Slices 35% BRAMs)	19 bit	167MHz	32 bit	2	16,7	0,6
XCV2000E	-6	55 MHz	(34% Slices 17% BRAMs)	19 bit	167MHz	32 bit	1	17,1	1,3
XCV800	-4	33 MHz	(72% Slices 100% BRAMs)	19 bit	167MHz	32 bit	1	10,3	1,3

- Core includes logarithmic (dual) 19/32bit ALU and A/D D/A conversion to 16/24bit I/Os
- Designed for Celoxica DK1 Handel C or standard VHDL/Schematic-based projects.
- Bit exact emulation libraries for Matlab/Simulik, MSVC and Handel **C** under Celoxica DK1.



Available as: *EDIF Macros + Bit-exact models. EDIF for Virtex, Virtex E, Virtex 2 and Virtex Pro.* **Precision:** *LNS: 19/32bit. Int2log, log2int: 16/24bit.* **Cost:** *Please, contact us. We provide the bit-exact Matlab/C/DK1 evaluation models for free. For the currently available downloads see:* http://www.utia.cas.cz/ZS/projects/hsla	**Contact:** Jiri Kadlec Department of Signal Processing Institute of Information Theory and Automation Prague, Czech Republic tel. +420 2 6605 2216 fax +420 2 6605 2511 kadlec@utia.cas.cz http://www.utia.cas.cz/ZS