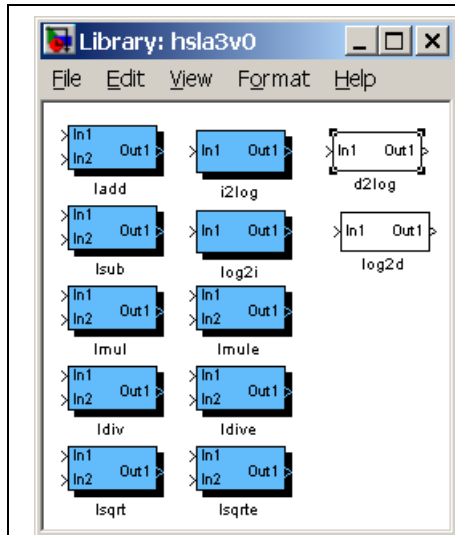# Logarithmic dual pipelined ALU Macros 19-bit and 32-bit

- ADD and SUB in **9 cycles.** MUL, DIV, SQRT in **2 cycles** in simple distributed macros.
- 19-bit ALU is using   8 Virtex BRAMs. Includes **int2log** and **log2int** conversion for 16-bit integers.
- 32-bit ALU is using 98 Virtex BRAMs. Includes **int2log** and **log2int** conversion for 24-bit integers.
- For design of SoC applications, requiring the floating point like data range and precision.
- Designed for Celoxica DK1 Handel C or standard VHDL/Schematic-based projects.
- Bit exact emulation libraries for Matlab/Simulik, MSVC and Handel **C** under Celoxica DK1.
- The 32-bit ALU provides the same data range/precision as the 32-bit floating point.
- ALU performance in DSP application (RLS Lattice filter) compared to TI C6711 FP processor:
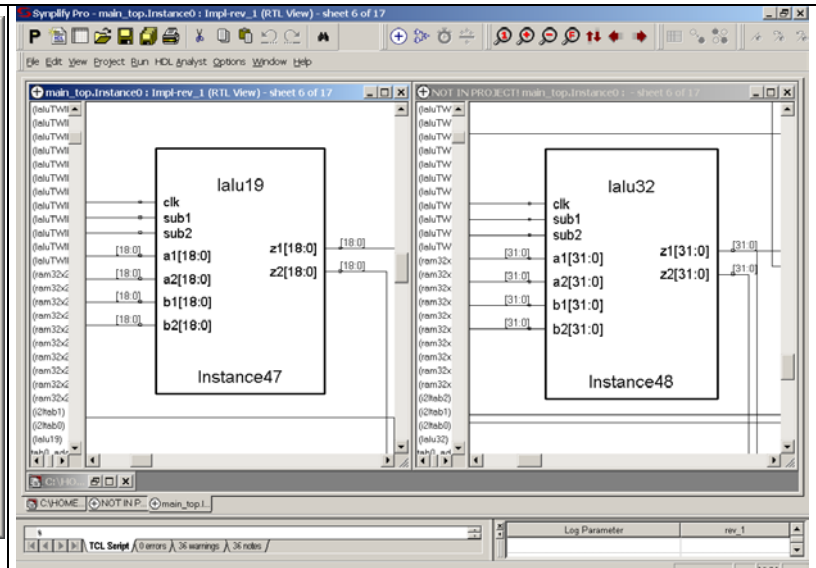
| Comparison of the maximal sampling frequency (RLS Lattice order 252) | | | | | No. of chan. | XILINX Virtex (kHz) | TI C67 (kHz) |
|---|---|---|---|---|---|---|---|
| *Virtex (Celoxica DK1-VHDL-ISE4.2i flow) ALU* Type      grade  clock      resources used | | | *TI C67:* Clock | *Float* prec. | | | |
| XC2V2000 -6  84 MHz (90% Slices  73% BRAMs) | | 32 bit | 225MHz | 32 bit | 1 | 26,1 | 1,7 |
| XCV2000E -6  45 MHz (55% Slices  76% BRAMs) | | 32 bit | 167MHz | 32 bit | 1 | 13,6 | 1,3 |
| XCV2000E -6  52 MHz (67% Slices  35% BRAMs) | | 19 bit | 167MHz | 32 bit | 2 | 16,7 | 0,6 |
| XCV2000E -6  55 MHz (34% Slices  17% BRAMs) | | 19 bit | 167MHz | 32 bit | 1 | 17,1 | 1,3 |

| Example of use in Handel C DK1 flow: | `ram int 32 a[16], b[16], result[16];`<br>`ladd1(a[i],b[j],result[k]);//in 9 cycles:result[k]=a[i]+b[j];` |
|---|---|



HSLA 3.0.0 bit-exact library for Matlab, Simulink, MSVC, DK1.1 (19/32 bit).

Synplicity Synplify 7.1 Analyst:   **alu19** and **alu32.**      Macros in use.