Application Note

Akademie věd České republiky
Ústav teorie informace a automatizace AV ČR, v.v.i.

Video Input/Output IP Cores for TE0820 SoM with TE0701 Carrier and and Avnet HDMI Input/Output FMC Module

Lukas Kohout, Jiri Kadlec, Zdenek Pohl
kohoutl@utia.cas.cz kadlec@utia.cas.cz xpohl@utia.cas.cz

Revision history

Rev.	Date	Author	Description
0	04.10.2019	L. Kohout	Initial version of the document
1			
2			

Contents

Acknowledgement

This work has been partially supported from project FitOptiVis, project number ECSEL 783162 and the corresponding Czech NFA (MSMT) institutional support project 8A18013.

1 Introduction

This application note describes video IP cores interfacing a video input and output of the Trenz TE0701-06 carrier board [1] with TE0820-3EG SoM (System on Module based on Xilinx Zynq UltraScale+) [2] and Avnet HDMI Input/Output FMC module [3]. The system is designed with Xilinx Vivado 2018.3 tool (Web Pack edition).

2 Description

This document describes two separate video chains in one system based on the Xilinx Zynq UltraScale+ device. The first video chain passes a video signal from the HDMI input through the frame buffer to the HDMI output. Both, HDMI input and output are provided by the Avnet HDMI Input/Output FMC module [3]. This video chain is supposed to be used for processing incoming video frames inside the FPGA and display the resultant video on the monitor. In the document, this video chain will be called *Primary Video Chain*. The second video chain consists of a frame buffer, dedicated video DMA and HDMI output on the TE0701-06 carrier board [1]. The frame buffer in this video chain is filled by ARM processor of the Zynq UltraScale+ processing system. It is supposed to be a desktop output of some operating system; PetaLinux kernel with Debian for instance. This video chain will be labeled as the *Secondary Video chain* in this application note. Figure 1 shows the top view of the system block design within the Xilinx Vivado 2018.3 tool.

2.1 Primary Video Chain

The primary video chain reads an input video signal from the HDMI input, stores the data from the video signal in the triple frame buffer and reads the data back to display them via HDMI output. It consists of 3 hierarchical blocks - HDMI Input, Video DMA Input/Output and HDMI Output. The input part of the chain can accept the video signal almost with every resolution, the upper limit is 1920x1080p60. The resolution of the output side of the chain is fully configurable up to 1920x1080p60.

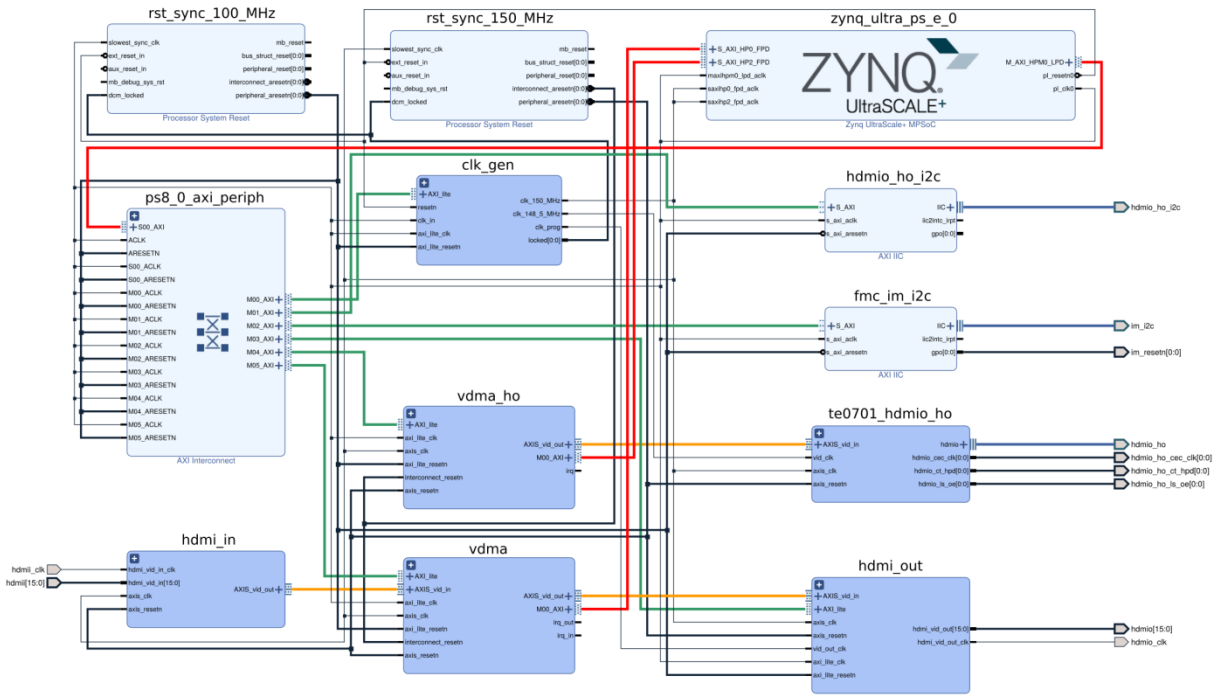

Figure 1: Block design of the whole system in Xilinx Vivado 2018.3 tool.

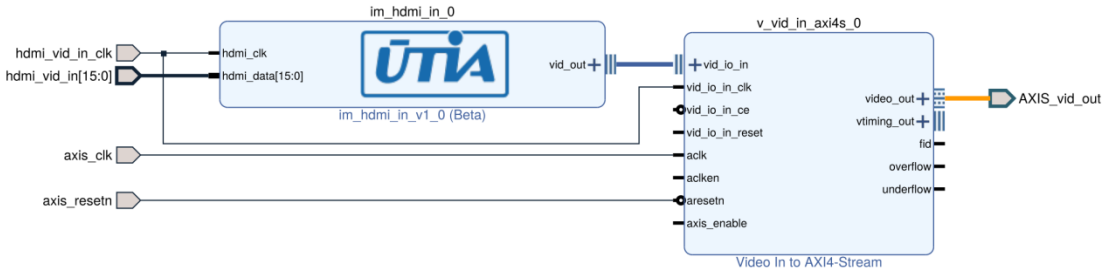

Figure 2: Primary Video Chain - HDMI Input.

2.1.1 HDMI Input

The HDMI input (*hdmi_in* block in Figure 1) converts an external video signal from the input HDMI codec on the Avnet HDMI FMC module to the AXI stream to pass the video data to the video DMA block. It includes two IP cores, see Figure 2.

- ***im_hdmi_in_0*** IP core reads the video signal in YCrCb 4:2:2 format. This signal includes embedded synchronization pulses. The core unpacks the syncs and provides complete video signal to its output. The core is developed by UTIA.
- ***v_vid_in_axis_0*** IP core converts complete video signal to the AXI stream. The stream is supplemented with signal *tuser*, which represents *start of frame*, and with signal *tlast*. The meaning of this signal is *end of line*. Optionally, this core provides a timing of the input video signal. This core is included as a standard part of the Vivado 2018.3 Web Pack tool.

2.1.2 Video DMA Input/Output

The Video DMA (*vdma* block in Figure 1) performs writing of the data from the input AXI stream to the main memory, and reading the data from the memory to feed the output AXI stream, the block includes two IP cores (see Figure 3).

- ***axi_vdma_0*** IP core is configured to have two independent DMAs. The first DMA reads the input AXI stream and writes its data do the frame buffer located in the main

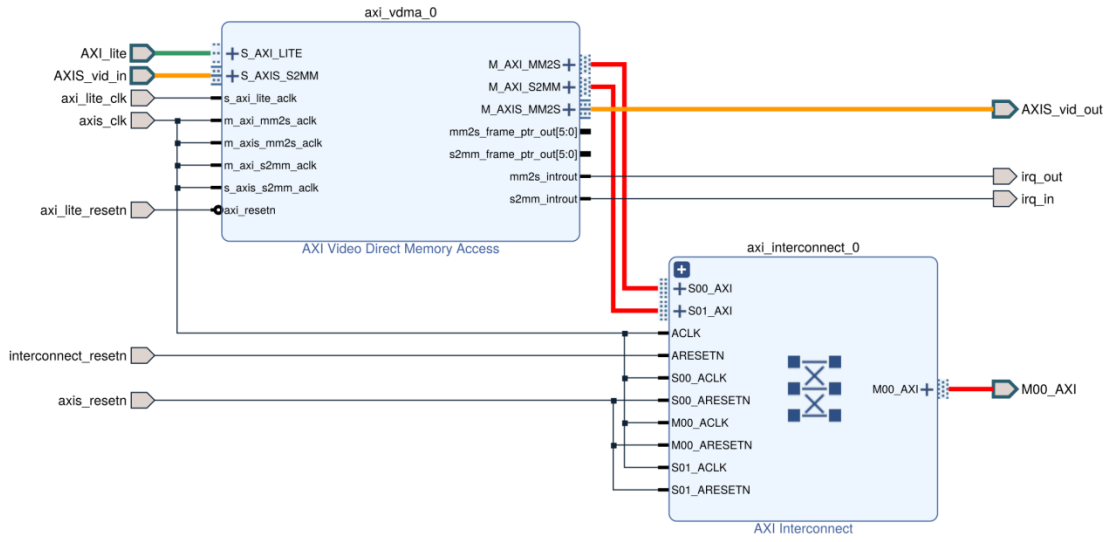

Figure 3: Primary Video Chain - Video DMA.

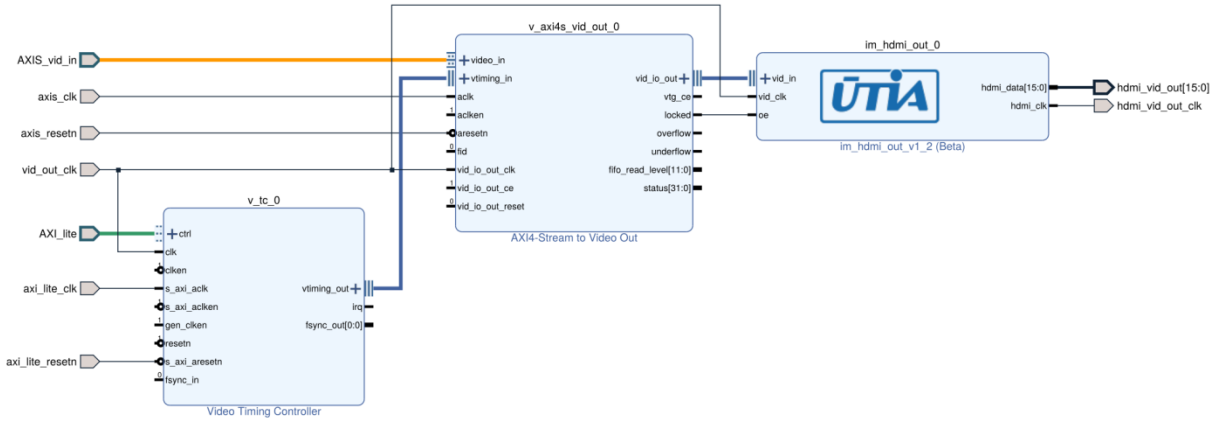

Figure 4: Primary Video Chain - HDMI Output.

memory. The second DMA reads the data from the frame buffer in the main memory and pushes the data to the output AXI stream. This block is configured to store 3 independent frames. It also provides an automatic internal lock among the frames to avoid image tearing. The core can be switched to the manual lock mode in SW application (parking mode) to process the locked frame and returns the resultant frame back to the frame buffer. This core is a part of the Vivado 2018.3 Web Pack.

- ***axi_interconnect_0*** core provides an interconnect between two AXI ports of the *axi_vdma_0* and one AXI high performance port of the Zynq UltraScale+ (its memory controller). This core is a part of the Vivado 2018.3 Web Pack.

2.1.3 HDMI Output

The HDMI output (*hdmi_out* block in Figure 1) converts an AXI stream from the video DMA block to the video signal which is processed by the output HDMI codec on the Avnet HDMI FMC module. The data of the video signal are coded in YCrCb 4:2:2 format. It is performed by 3 IP cores within the block, they are shown in Figure 4.

- ***v_tc_0*** IP core is a timing controller. It generates synchronization pulses according to required output video resolution and frame rate. This core is a standard part of the Vivado 2018.3 Web Pack.
- ***v_axis_vid_out_0*** IP core gets a video data from the video DMA block via AXI stream and synchronization pulses from the timing controller. It converts the data from the AXI stream to the complete video signal with respect to the required timing. This core is also available in the Vivado 2018.3 Web Pack.
- ***im_hdmi_out_0*** IP core converts a complete video signal with standalone synchronization pulses from the *v_axis_vid_out_0* core to the video signal containing embedded synchronization pulses. This video signal is required by the output HDMI codec on the Avnet HDMI FMC module. This core is developed by UTIA.

2.2 Secondary Video Chain

The secondary video chain consists of a frame buffer with corresponding video DMA and its own HDMI output. The video chain includes 2 hierarchical blocks – Secondary Video DMA Output and Secondary HDMI output. The resolution of the video signal processed in this video chain is fixed to 1920x1080p60.

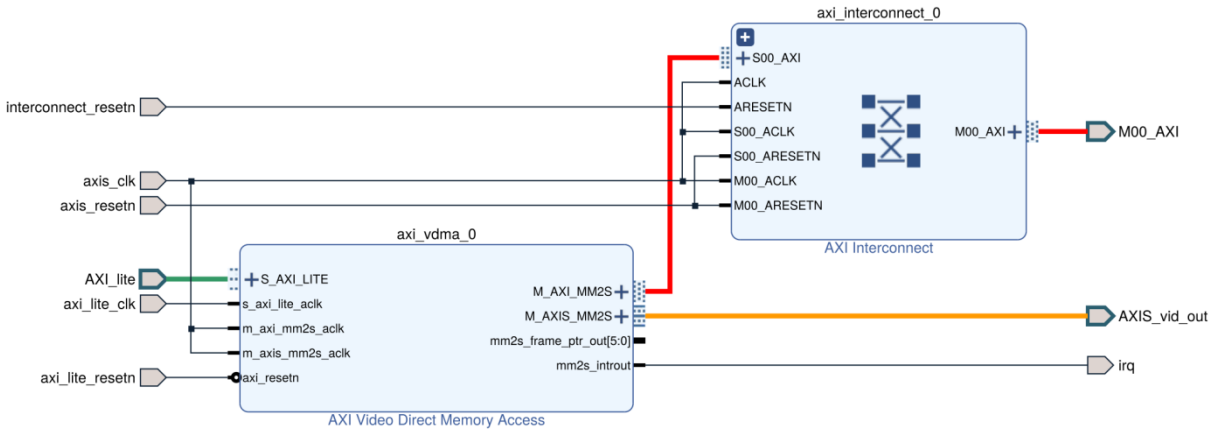

Figure 5: Secondary Video Chain - Video DMA.

2.2.1 Secondary Video DMA Output

The Secondary video DMA (*vdma_ho* block in Figure 1) performs reading of the data from the memory to push them to the output AXI stream. This block includes 2 IP cores (see Figure 5).

- ***axi_vdma_0*** IP core is configured to have only output DMA. It reads the data from the frame buffer in the main memory and pushes the data to output AXI stream. This block is configured to store single frame in the frame buffer. The format of the data in the frame buffer is ABGR. The reason of this is a possibility to use it as an output screen of some linux desktop using a simple-framebuffer driver (PetaLinux kernel with Debian distribution for example). This core is included in the Vivado 2018.3 Web Pack.
- ***axi_interconnect_0*** IP core provides an interconnection between AXI port of the *axi_vdma_0* and AXI high performance port of the Zynq UltraScale+ (its memory controller). This core is a part of the Vivado 2018.3 Web Pack.

2.2.2 Secondary HDMI output

The secondary HDMI output (*te0701_hdmio_ho* block in Figure 1) converts an AXI stream from the secondary video DMA block to the video signal which is provided by the output HDMI codec on the TE0701-06 carrier board. The data of the output video signal are coded

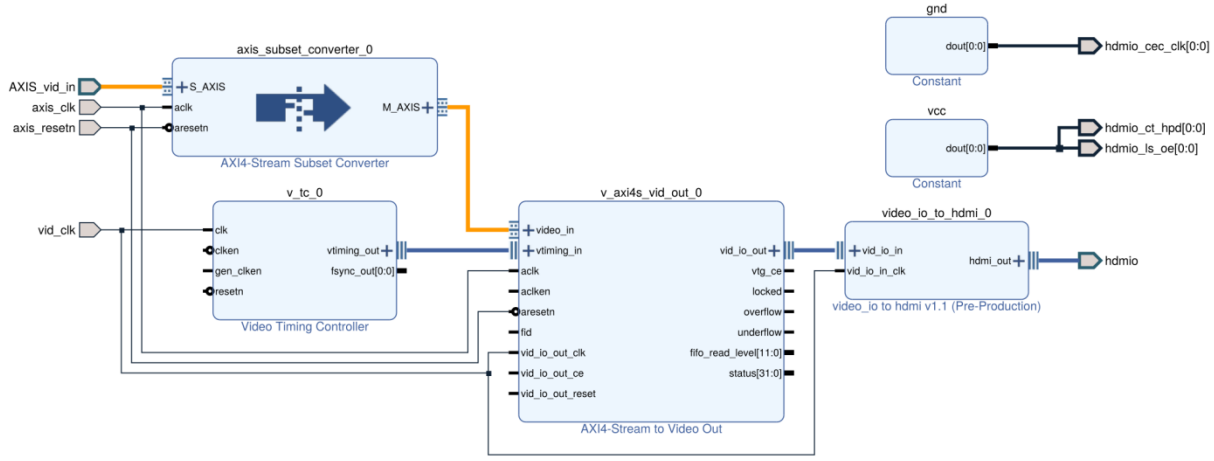

Figure 6: Secondary Video Chain – HDMI Output.

in RGB format. It is performed by 4 IP cores within the block, they are shown in Figure 6. The block also contains two cores generating logic constants ’0’ and ’1’.

- ***v_tc_0*** IP core is a timing controller. It generates synchronization pulses according to 1920x1080p60 video resolution. This core is a standard part of the Vivado 2018.3 Web Pack.
- ***axis_subset_converter_0*** IP core reads video data from the Secondary video DMA (its output AXI stream) and converts them from ABGR video format to RGB. It is required by HDMI codec on the TE0701-06 carrier board. This core is a part of the Vivado 2018.3 Web Pack.
- ***v_axis_vid_out_0*** IP core gets video data from the *axis_subset_converter_0* block via AXI stream and synchronization pulses from the timing controller. It converts the data from the AXI stream to the complete video signal with respect to the required timing. This core is also a part of the Vivado 2018.3 Web Pack.
- ***video_io_to_hdmi_0*** IP core converts a complete video signal with standalone synchronization pulses from the *v_axis_vid_out_0* to the DDR form. This video signal is required by the output HDMI codec on the TE0701-06 carrier board. This core had been originally developed by Trenz Electronic, the current version of the core has been modified by UTIA to support Zynq UltraScale+ device.

2.3 Auxiliary Cores

Primary and secondary video chains need other auxiliary cores to run (see Figure 1). All of them are available in Vivado 2018.3 Web Pack tool.

- ***fmc_im_i2c*** and ***hdmio_ho_i2c*** are I^2C controllers used for configuration HDMI codecs on the Avnet HDMI FMC module and TE0701-06 carrier board. Both are configured to 100 kHz speed.
- ***clk_gen*** is a hierarchical block including 3 clock generators. The first, it generates 150 MHz clock driving AXI streams. The second, it generates a fixed pixel clock for the secondary video chain, the frequency is 148.5 MHz. The third clock generator is configured to be programmable from the software application, its output clock is used as pixel a clock of the primary video chain.
- ***ps8_0_axi_periph*** IP core provides an interconnection among all AXI-Lite interfaces and Zynq UltraScale+. AXI-lite interface is used for configuring internal registers of IP cores.

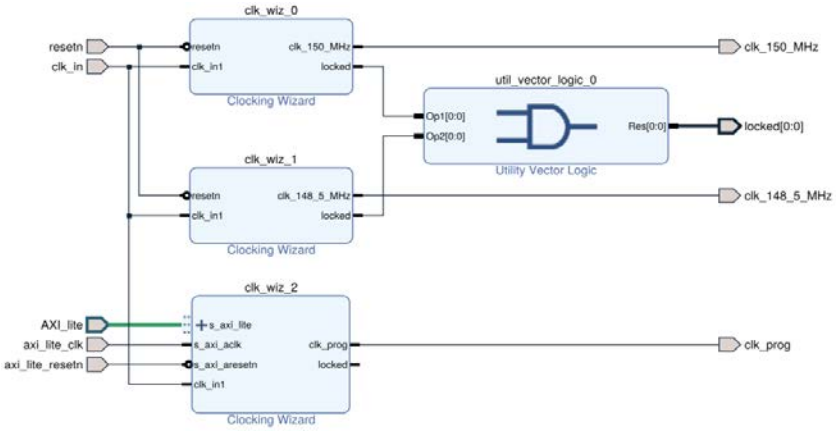

Figure 7: Clock generator.

- ***rst_sync_100_MHz*** and ***rst_sync_150_MHz*** cores perform synchronous resets for other cores, *rst_sync_100_MHz* is synchronous with 100 MHz clock driving AXI-Lite interfaces, *rst_sync_150_MHz* is synchronous with 150 MHz clock driving AXI streams.
- ***zynq_ultra_ps_e_0*** IP core encapsulates complete Zynq UltraScale+ processing system.

3 Required Hardware

The list bellow summarizes required HW components to run the demonstrator.

- Trenz Electronic TE0820-3EG SoM [2]. It consists of the Xilinx Zynq UltraScale+ XCZU3EG-SFVC784-1-E device and 2 GB DDR4 memory. The Zynq UltraScale+ device is quad core ARM A53, dual core ARM Cortex R5 and programmable logic area on a single 16 nm chip. The PCB of the module has the 4x5cm form factor, the board is designed and manufactured by company Trenz Electronic [2]. A very similar module can be seen in Figure 9.
- Trenz Electronic TE0701-06 carrier board [1]. It expands IOs of the SoM, it provides different types of connectors such as PMODs, FMC low pin count connector, HDMI output, SD Card slot and so on. The carrier can be seen in Figure 8.

Figure 9: TE0820-3EG SoM [2], the figure shows a similar product.

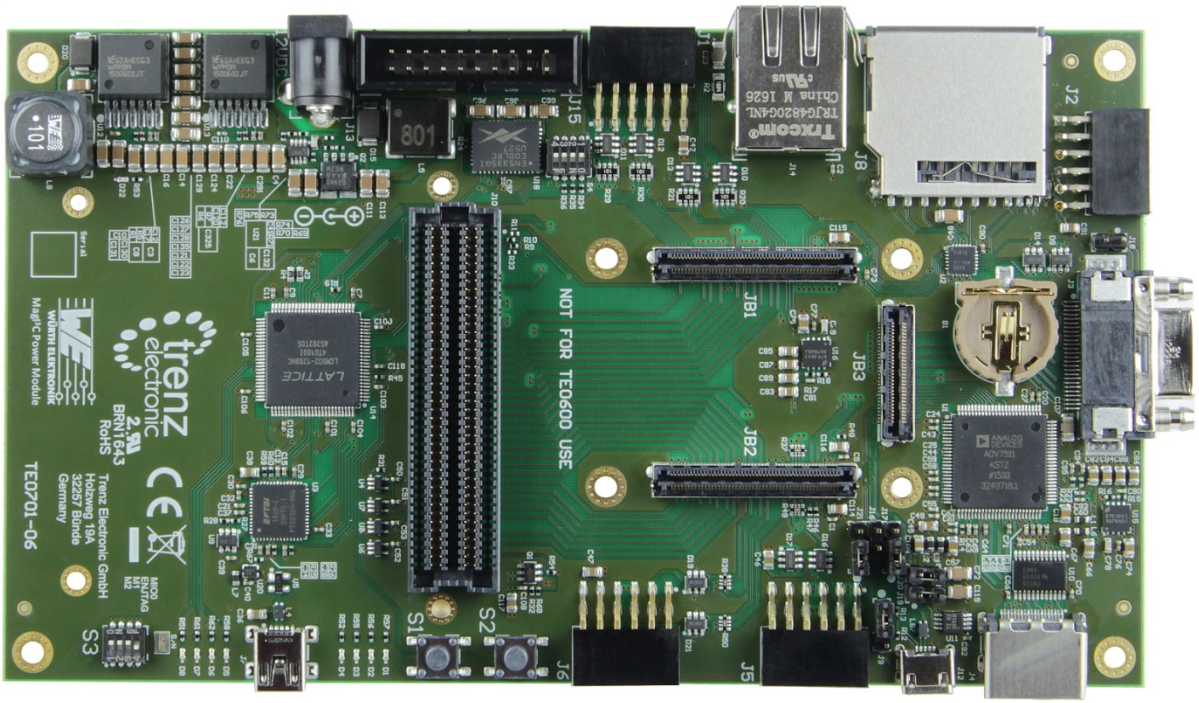

Figure 8: TE0701-06 [1].

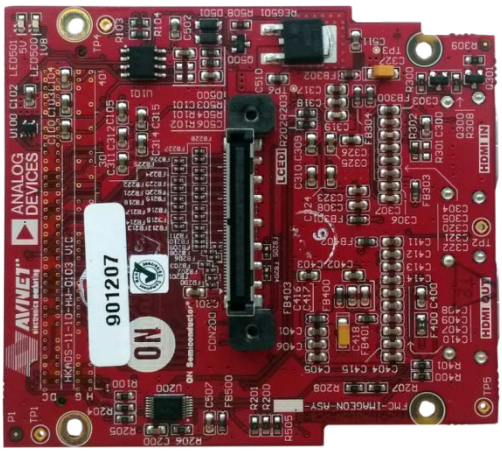

Figure 10: Avnet HDMI Input/Output FMC Module [3].

- Avnet HDMI Input/Output FMC Module [3]. It provides HDMI input and HDMI output interfaces in YCrCb 4:2:2 format with embedded synchronization pulses. Figure 10 shows the top view of the FMC card.

4 SW Application

The application uses a serial terminal to communicate with a user. The settings of the terminal are summarized in Table 1. After the application startup is finished and all cores are configured, the application prints its menu on the serial terminal screen. The menu is presented in Table 2. The application demonstrates both, primary and secondary video chains ability.

Table 1: Serial terminal settings.

Parameter	Value
Speed	115200
Data bits	8
Stop bits	1
Parity	None
Control Flow	None

Table 2: Application menu.

Key	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, a	Set output resolution of the primary video chain. Choices: 1920x1080p60, 1920x1200p50, 1600x1200p50, 1680x1050p60, 1280x1024p60, 1280x720p60, 1024x768p60, 800x600p60, 640x480p60, 600x800p60
l	Shift output image of the primary video chain to the left by 4 pixels.
r	Shift output image of the primary video chain to the right by 4 pixels.
d	Shift output image of the primary video chain down by 1 line.
u	Shift output image of the primary video chain up by 1 line.
z	Set the image position to point [0, 0].
c	Change the background color in the frame buffer of the secondary video chain
m	Print this menu
x	Exit the application

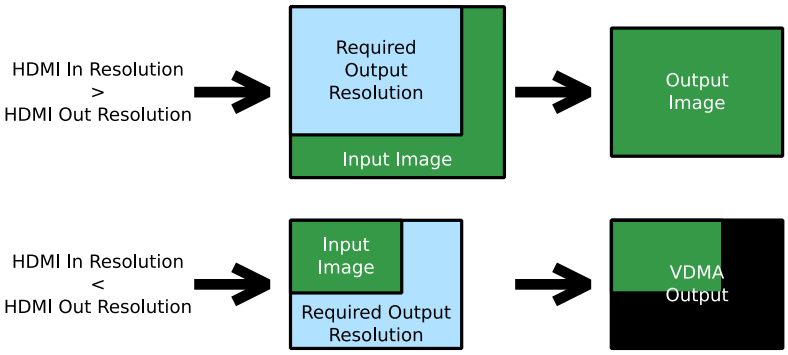

Figure 11: Behavior of the VDMA in the primary video chain demo when the input resolution is not the same as the output resolution.

4.1 Primary Video Chain Demonstration

The primary video chain demonstrator is a video pass through demonstrator. The video signal originates from the HDMI Input on the Avnet FMC module, it is stored in the video frame buffer. After that it is read from the frame buffer and drives to Avnet HDMI Output part of the FMC module. Table 3 summarizes supported input video signal resolutions as they are presented by EDID to the input video signal source (PC graphic card). The output resolution can be changed on the fly, supported resolutions are presented in Table 2. If the resolution of the input video signal is less than the output resolution, the whole input video image will be displayed with additional black frame to comply the output resolution. In case that the resolution of the input video signal is greater than the output resolution, the output will be created by cropping of the input video signal. This behavior is shown in Figure 11. In this case the image can be also shifted to left, to right, up and down.

4.2 Secondary Video Chain Demonstration

The secondary video chain is fixed to 1920x1080p60 resolution. Its frame buffer is filled by the ARM processor, the user can change a background color. The frame buffer content is displayed on the monitor via HDMI output port on the TE0701-06 carrier board.

Table 3: Primary video chain HDMI Input EDID - supported input resolutions.

Resolution	Frame rate
1920x1080	60
1680x1050	60
1600x1200	50
1440x900	60
1366x768	60
1280x1024	60
1280x960	60
1280x800	60
1280x720	60
1152x864	60
1152x720	60
1024x768	60
800x600	60
800x480	60
720x576	60
720x480	60
640x480	60

5 Demonstrator Startup

To run the demonstrator follow the steps bellow.

1. Connect the TE0701-06 HDMI output to the monitor capable of displaying Full HD resolution at 60 frames per second (1920x1080p60).
2. Connect the Avnet HDMI output to monitor capable of displaying Full HD resolution at 60 frames per second (1920x1080p60).
3. Connect a valid video signal to the Avnet HDMI input (output from the PC graphic card for instance). Table 3 summarizes all resolutions presented by EDID.
4. Connect a micro USB cable to J7 connector on TE0701-06 carrier board (JTAG/USB-to-Serial). Serial terminal settings:
    - Baud rate – 115200
    - Data bits – 8
    - Stop bits – 1
    - Parity – none
    - Flow control – none
5. Copy file *BOOT.bin* to the root of the SD card, see the content of attached package in Section 6. Insert the SD card to the slot on the TE0701-06 carrier board.
6. Power the board on (12 V).
7. Observe the serial terminal to see the application prints and to control the demonstrator.

To obtain all demonstrator source codes, do not hesitate to contact UTIA partner at contact e-mails kadlec@utia.cas.cz or kohoutl@utia.cas.cz.

6 Package Content

```
.
├── doc
└── prebuilt
    └── BOOT.bin
```

7 References

[1] Trenz Electronic, „TE0701 Carrier Board TRM,“ 13 06 2018. [Online]. Available: http://www.trenz-electronic.de/fileadmin/docs/Trenz_Electronic/Modules_and_Module_Carriers/4x5/4x5_Carriers/TE0701/REV06/Documents/TRM-TE0701-06.PDF.

[2] Trenz Electronic, „TE0820 TRM,“ 18 08 2019. [Online]. Available: http://www.trenz-electronic.de/fileadmin/docs/Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV03/Documents/TRM-TE0820-03.pdf.

[3] AVNET, „HDMI Input/Output FMC Module,“ 11 04 2019 [Online]. Available: https://www.avnet.com/shop/us/products/avnet-engineering-services/aes-fmc-hdmi-cam-g-3074457345635221625/.